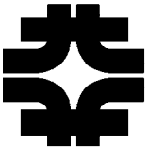


Fermi National Accelerator Laboratory

D-Zero Central Fiber Tracker
8-MCM Analog Front End Board

Design Specification

--PRELIMINARY--

January 7, 2000

John T. Anderson

1. GENERAL INFORMATION

This document describes the design of the Analog Front End Board (AFE), which has the function of receiving charge signals from the Central Fiber Tracker and providing digital hit pattern and 8-bit charge amplitude information from those charge signals. Two versions of the Analog Front End Board are being manufactured:

1. The 8-MCM AFE, which digitizes 512 channels of information and provides one bit of discriminator data per input;
2. The 12-MCM AFE, which digitizes 512 channels of information, and provides one bit of discriminator data for each of 256 of the channels, and two bits of discriminator data (dual threshold) for the other 256 channels.

Since the 12-MCM AFE is a very different animal than the 8-MCM AFE, both in terms of data structure and physical structure, it will be mentioned in this document only where both boards have identical function. A separate document, cloned from this one, will describe the 12-MCM AFE in full detail.

1.1. System Introduction

The CFT system consists of a set of 8 concentric cylinders of optical fiber arranged in layers. Each of these layers has 'axial' fibers, that is, those which run parallel to the beam direction; there are also 'stereo' fibers, which wrap in gentle helices around the beamline. Half of the 'stereo' fibers have a clockwise twist, and the other half have a counter-clockwise twist, such that data from a correlated clockwise and counter-clockwise pair of hits indicates a distance from the interaction point along the beam axis.. The 360 degrees of rotation around this axis have been broken into 80 'sectors', each of which spans 4.5 degrees. Each AFE board is connected to one sector's worth of fibers. Two boards are installed into a mechanical 'cassette', which views a total of 1024 fibers. The mechanical design of the cassette requires that the two boards be on opposite sides; part height clearances require that both boards face 'away' from the centerline of the cassette. This has resulted in the concept of 'right-handed' and 'left-handed' boards, indicative of the direction in which the components protrude away from the cassette centerline when viewed from the front. Analysis of the AFE boards has resulted in the realization that a single 'non-handed' design – that is, a single layout which can be used in both orientations- is possible, so long as certain minor restrictions in the fiber placement at the top of the cassette are observed.

Each successive layer of fibers from innermost ('A') to outermost ('H') has more fibers than the last; in addition, an eighth layer of Preshower ('PS') fibers exists outside the H layer. Preshower fibers are larger than the axial fibers; there are relatively few PS fibers per sector, but triggering requirements force a different circuit design for PS fibers as opposed to axial fibers. Every PS fiber is measured twice, at two different thresholds; also, the thresholds associated with the PS fibers are sufficiently different from the axial fibers that the entire PS circuit must be independent of any axial fiber circuit. This places limits on the distribution of fibers into the AFE boards.

Each sector of information from the detector consists of 512 'axial' fibers and an additional 512 'stereo' fibers. Each sector contains

- 32 'A' layer fibers
- 40 'B' layer fibers
- 48 'C' layer fibers
- 56 'D' layer fibers
- 64 'E' layer fibers
- 72 'F' layer fibers
- 80 'G' layer fibers
- 88 'H' layer fibers
- 32 'PS' layer fibers

Only the 'axial' fibers are used in trigger formation, so all 'axial' fibers are routed into one set of AFE boards and all 'stereo' fibers are routed into different AFE boards. The Preshower is handled separately so there are 480 axial fibers per sector required to form the trigger. A second complication is that the Preshower fibers are further broken up along the beamline axis; at any given spot around the cylinder, the single Preshower location of that angle has three Preshower fibers – a Forward North, a Central, and a Forward South. To accommodate the dual threshold measurements required of Preshower fibers, the 12-MCM version of the AFE is used where eight of the twelve measurement blocks are utilized as four dual-threshold devices. The remaining four measurement devices are then used as single-threshold objects for some of the 'stereo' fibers. The remaining 'stereo' fibers, plus all of the 'axial' fibers, are handled by the 8-MCM AFEs, which have eight identical single-threshold measurement blocks. This arrangement is shown in Figure 1.

Note that in figure 1, some 30 boards are marked with an asterisk (*). This indicates that these 30 boards are called out twice in the diagram because they handle fibers from two different sections of the detector. The actual board total is 75 + 32 + 60 + 30 = 197 boards. Of these, 52 are the 12-MCM variety and the remaining 145 are the 8-MCM version.

For further details of the detector arrangement, please access the detector pages on the web. A reasonable starting point is
http://D0server1/Projects/TriggerElectronics/WebDocs/Trigger_index.htm

For the purposes of this document, it is sufficient to note that all the fibers from the detector are landed into either 8-MCM or 12-MCM boards, and that all 512 channels of the 8-MCM AFE are single-threshold. In the 12-MCM variation, 256 channels are single threshold while the other 256 are dual-threshold.

All channels of analog data seen by the AFE boards pass through discriminators. Each discriminator creates one bit of data per input channel, creating a bitmap of fibers whose charge was above threshold. This pattern is sent to Digital Boards every crossing of the beam (every 132 nsec) by high-speed serial data links. There is a single Digital Board for every pair of AFE boards used in track finding. These Digital Boards take the bit pattern of which fibers were above or below threshold to find particle tracks. To obtain sufficient bandwidth, each 8-MCM AFE board must drive four digital links to a given Digital Board.

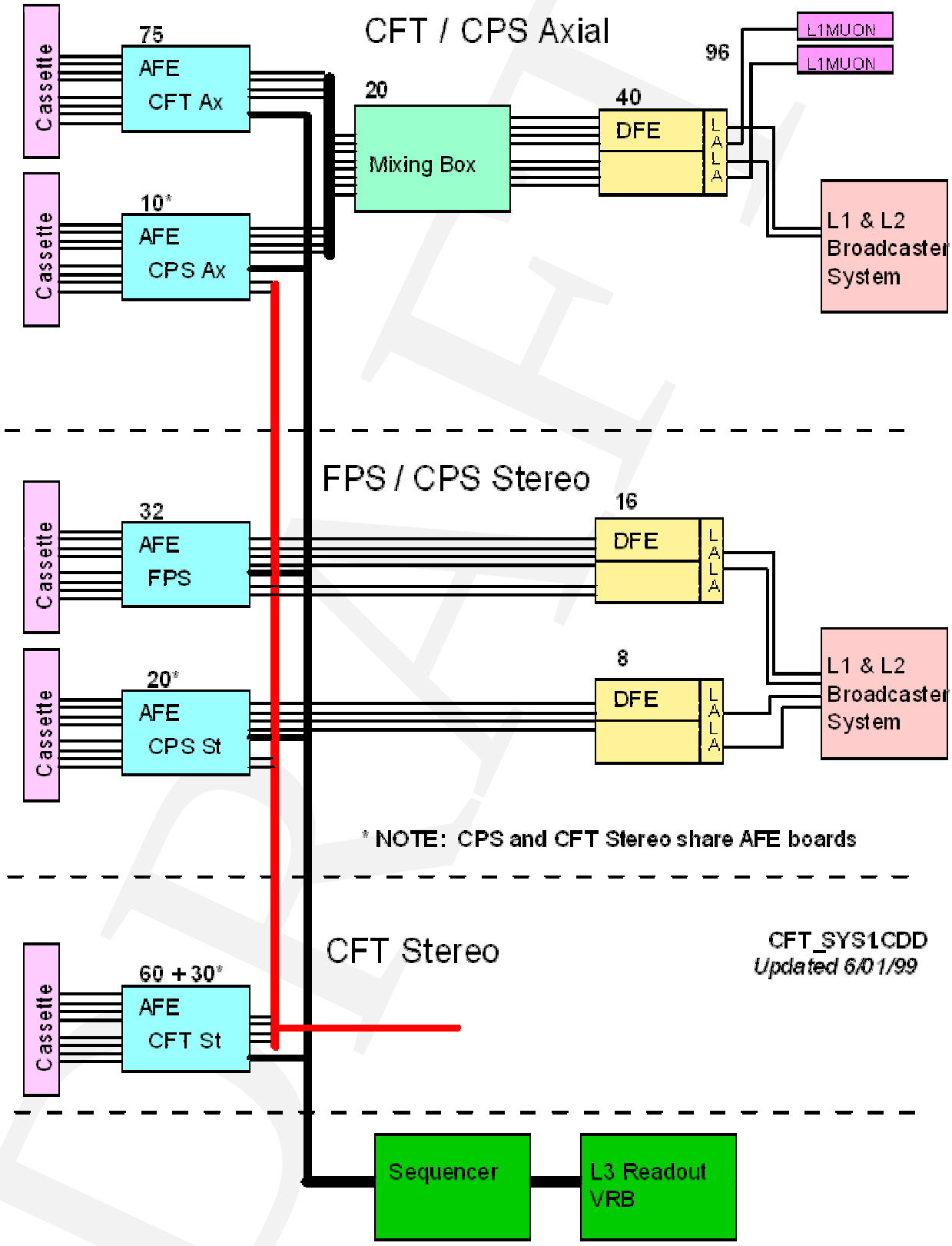

CFT / CPS Axial
Cassette
75
AFE
CFT Ax
Cassette
10*
AFE
CPS Ax
20
Mixing Box
40
DFE
LALA
96
L1MUON
L1MUON
L1 & L2
Broadcaster
System
FPS / CPS Stereo
Cassette
32
AFE
FPS
16
DFE
LALA
Cassette
20*
AFE
CPS St
8
DFE
LALA
L1 & L2
Broadcaster
System
* NOTE: CPS and CFT Stereo share AFE boards
CFT Stereo
CFT_SYS1CDD
Updated 6/01/99
Cassette
60 + 30*
AFE
CFT St
Sequencer
L3 Readout
VRB

Figure 1

1.2. Description Of Component & How It Fits Into The System

The 8-MCM AFE board is a multilayer printed circuit board which is 9U (14.435 inches) high and 19.25 inches deep. Each AFE slides into guide rails in a mechanical cassette which houses the light-to-charge conversion circuitry. As the AFE is installed into the cassette, it plugs into a backplane from which it derives power and control connections. After insertion into the cassette, a set of flexible circuit cables is connected to the AFE along the bottom edge to deliver the analog input signals.

The cassette is a complex mechanical assembly. One AFE is mounted on each side of the cassette. Each AFE has its components on the outside, so the AFE must be mirror-imageable left to right so that it may be plugged into either side of the cassette. The cassette electronics requires operation at cryogenic temperatures, so relatively long and specially designed cables bring the low-level analog signals from the bottom of the cassette (held at about 9 Kelvin) to the room-temperature AFE.

1.3. List Of Component Requirements

- Mirror-image left to right design
- Mechanically compliant with cassette design
- Must accept 512 low-level charge signal inputs
- Must discriminate all 512 channels every 132 nsec
- Must deliver digital result of all 512 channels to Digital Boards and/or Mixer System every 132 nsec via multiple high-speed LVDS links
- Relatively low power (~40 Watts) due to limited airflow
- Controlled by MIL-STD 1553 interface
- Able to provide test pattern data in lieu of real data
- Interfaces to SVX Sequencers for readout of SVX chips when discriminator pattern is indicative of interesting event
- Buffers all discriminator data for redundant readout of discriminator pattern that caused trigger over SVX bus when SVX chips read out
- Able to act as closed-loop temperature controller for cryostat photoelectronics
- Provide all required clocks to control SIFT discriminator chips

2. THEORY OF OPERATION AND OPERATING MODES

2.1. Basic Features & Operation

The 8-MCM AFE contains a number of subsystems. Figure 2, on the next page, gives the overview. The essential subsystems are as follows:

- Interface to MIL-STD 1553
- Dual-port RAM between 1553 interface and internal microprocessor
- Microprocessor with built-in A/D converter
- DAC system to develop all control voltages for SIFT chips in the MCMs
- A clock generation system to develop all required timing clocks for the SIFT chips
- Eight Multi-Chip Modules (MCMs) that perform measurment of the analog signals
- A 'Virtual SVX' (VSVX) system to buffer discriminator data for readout with SVX data
- An interface to the SVX Sequencer for SVX control and readout
- Analog monitoring for the cassette temperature and VLPC bias control
- High speed data multiplexing system which takes all discriminator data from the SIFT chips and sends it via LVDS links to the Digital Boards.

The heart of the AFE is eight Multi-Chip Modules (MCMs) which each contain four SIFT discriminator chips and one SVX II charge-sensitive ADC. Each MCM can 'see' up to 72 channels of charge input. Every 132 nsec the SIFTs provide one bit of discriminator output per channel, where a '1' indicates that the charge delivered to the SIFT was above a threshold set by a control voltage. The charge collected by each channel of each SIFT is transferred using a switched-capacitor charge pump to an SVX II chip such that the entire event is stored in the analog pipeline of the SVX. Should the discriminator pattern of this and all other trigger AFE boards indicate an interesting event, the Level 1 Trigger initiates a readout of the SVX II chips in all the AFEs, which provide 8-bit digitization of the stored charges, providing analog readout of the same charge pattern that caused the trigger in the first place.

2.2. Diagnostic Features

Numerous diagnostics are built into the AFE:

- The microprocessor can read back all the DAC settings and verify the DACs are working.
- The microprocessor can exercise the dual-port RAM
- The microprocessor can 'snoop' on SVX data readout and/or insert test data into the SVX data readout; this also allows redundant readback of SVX and VSVX data over the 1553 bus
- The MIL-STD 1553 interface provides read/write loopback capability for testing the interface from the remote computer

- All major logic functions are provided using in-system programmable logic devices.
- The CPLDs which read out the SIFT chips can insert test patterns into the LVDS readout to the Digital Boards
- Cryostat temperature, board voltages, board temperature and other analog parameters can be continually monitored by the microprocessor and reported to online systems via the 1553 interface.

2.3. MIL-STD 1553 Interface

The MIL-STD 1553 serial link is used as the main control connection to the AFE board. Each AFE has its own Remote Terminal (RT) interface which implements the required timing. To the 1553 system, each AFE implements only two subaddresses, typical subaddresses 16 and 17 (0x10 and 0x11). Each board appears to be a 2K X 16 RAM where subaddress 16 is the address in the RAM where data is read/written, and subaddress 17 is the port where the data is read or written.

A few locations in the RAM are reserved as a 'command queue' which is loaded by the 1553 controller with eight-bit command values. The queue is filled with commands and, when the list is ready, a terminal value is written to a different address which causes the on-board microprocessor to implement the list of commands previously stored. The rest of the RAM is allocated to status information and board settings. All RAM locations are available to the 1553 interface, which may interrogate them at any time.

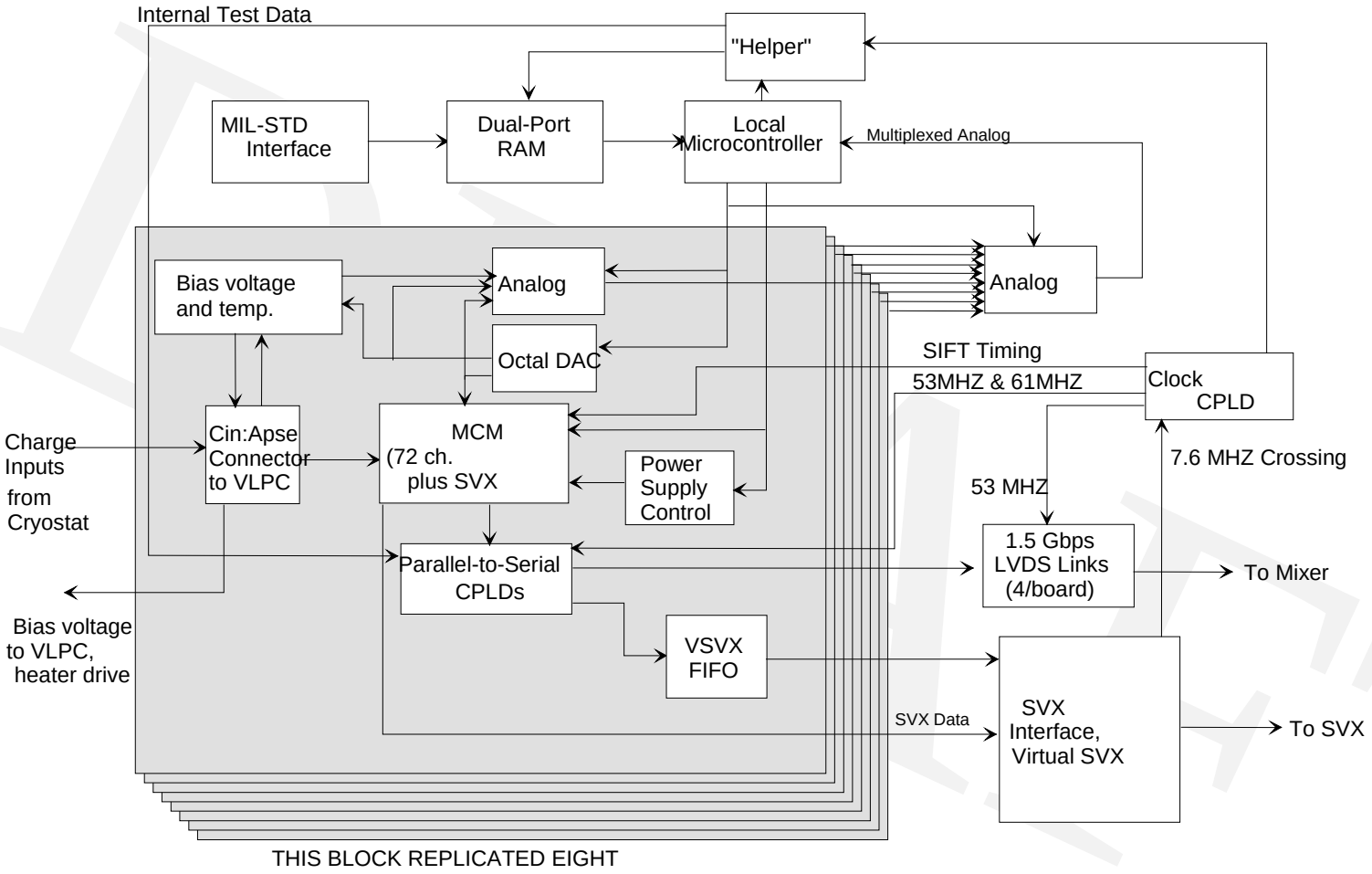
All commands and their interpretation are controlled by the firmware of the on-board microprocessor, which is EPROM based and thus cannot be changed by the end user. Engineering note A980922A, at

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a980922a.pdf

provides a detailed look at the memory map of the board. This note is somewhat dated and will be rewritten in the near future.

The 1553 interface of the AFE is compatible with the VME-to-1553 interface used elsewhere in D-Zero, originally designed by the Accelerator Division Controls group. This board is often used for testing and will probably be used in testing the AFE. The necessary software information to use this VME interface to 1553 may be found at

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990312a.pdf



CFT Axial Analog Front End

Figure 2

2.4. Dual-Ported RAM

All accesses to the AFE from the 1553 bus load data into or read data from a dual-ported 2K X 16 RAM. Since the internal microprocessor uses an eight-bit bus, the RAM on the microprocessor side is organized as 4K X 8. The dual-port architecture allows this bus width change and also allows simultaneous access from both sides, simplifying any collision detection. The microprocessor side of the RAM is subservient to the 1553 side, such that if the micro tries to access the same location as is currently addressed by 1553, the micro will receive a BUSY signal and must wait it's turn.

Any 16-bit value written to the DPRAM by the 1553 interface is presented to the micro as two bytes at adjacent addresses; however, since there are twice as many microprocessor addresses, the address from the micro side is double the address from the 1553 side Thus, the 16-bit address 0x35 from the 1553 side is the same data as the two bytes at addresses 0x6A and 0x6B. The current addressing convention is that the even address from the micro side is bits 7:0 of the data from the 1553 side, and the odd address is bits 15:8.

2.5. Microprocessor

A Microchip PIC 14000 microcontroller is used on the AFE. The PIC 14000 is chosen because it combines a fairly large code space (4K words), internal A/D converter, reasonable clock speed and integrated I^2C bus support into one package. The microprocessor provides supervisory and diagnostic control functions in the AFE but in no way interferes with the high-speed data acquisition functionality. The basic jobs handled by the micro are the following:

- Poll the dual-port RAM and respond to commands from the 1553 bus;
- Load analog control voltages to the DAC subsystem over the I^2C bus;
- Perform analog readback of DAC voltages, board temperature, board power supply voltages and cryostat temperature using its internal A/D converter;
- Sequence the power supply turn-on and turn-off to the SVX and SIFT chips;
- Act as local closed-loop temperature controller for the VLPC chips in the cassette.

The microprocessor firmware is coded entirely in assembly language and is not available to the end user once installed in the AFE. The chip itself is EPROM-based which allows changes to the firmware, but only if access to the AFE board itself is possible. Remote downloads of firmware are not supported.

A 'helper' CPLD demultiplexes the microprocessor I/O lines and provides the necessary support to address the dual-port ram, and write/read the various internal registers of the board. Most internal registers are not made directly accessible to the end user but instead are manipulated in fixed fashion in response to command codes sent to the micro by the end user. This insures that only known working sequences of register operations ever occur.

The microprocessor clock is derived from the on-board 1553 interface clock, so that the micro will run even if the AFE is disconnected from the rest of the fiber tracker system.

2.6. DAC Subsystem

Each of the eight multi-chip modules (MCMs) in the AFE require numerous analog control voltages to function:

- For each of the four SIFT discriminator chips within the MCM (each SIFT handles 18 of the 72 channels within the MCM), there is a threshold voltage which determines the required charge for the discriminator to yield a '1'. Due to vagaries in the SIFT design the threshold is actually the difference between two voltages that have a common-mode point of 2.5 volts; this, however, is hidden from the user by the use of a couple of op-amps that derive the companion voltage from the DAC setting.
- For each of the four SIFT discriminator chips within the MCM there is also a reference voltage V_{REF} which controls the pedestal and dynamic range of the charge transfer from the SIFT to the SVX II chip used as the 8-bit A/D of the AFE.
- Each pair of SIFT chips also requires a dynamic range control voltage.
- There is also a charge transfer circuit clamp voltage V_{CLMP}, common to all four SIFTs in the MCM.

The dynamic range control and V_{CLMP} voltages may be supplied by simple resistor voltage dividers, but the other eight voltages must be variable. Thus, each MCM has associated with it an octal DAC. The nominal gain of the SIFT is about 30 fCoul per volt, with a maximum range of about 150 fCoul. Thus, with an eight-bit DAC, the threshold can be ideally set in 0.585 fCoul steps. However, offset differences between the SIFTs and noise will probably limit the resolution to 1-2 fCoul.

In addition to the eight octal DACs required to provide all of the MCM control voltages, each of the eight input cables from the cryostat to the AFE have some analog voltages associated with them:

- A bias voltage supply for the VLPC photodiodes;
- A constant current supply for the temperature sense resistor;
- A heater drive supply for the temperature maintenance resistor mounted adjacent to the VLPCs in the cryostat.

Two channels of DAC are assigned for each cable, one for the bias voltage and one for the heater supply. The constant current supply is fixed. Two octal DACs thus suffice for all eight cables, for a total of ten octal DACs (eighty DAC channels) across the board.

The I^2C bus addressing mechanism for the octal DAC parts allows for only four octal DACs on the bus, so a bus switching scheme is implemented that partitions the board into four I^2C sub-buses. Sub-buses 'A' and 'B' are used to control the eight MCMs, and sub-bus 'D' controls the cable voltages. Sub-bus 'C' is reserved for address expansion as will be required on the 12-MCM variant of the board. Further details of the DAC subsystem design may be found at

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990607a.pdf

This document is also undergoing some revision but is reasonably up to date.

2.7. Clock Generation

The AFE board must synchronize to the 7.6 MHz beam crossing clock as provided by the SVX Sequencer boards in order to correctly acquire the data. However, in order to transmit the data to the Digital Boards, a faster clock is required. A phase-locked loop is used to multiply the beam crossing clock by 7 to generate 53.104 MHz, the usual RF clock frequency found in Fermilab applications. This clock is also used as the data clock to the LVDS serial links which transmit the discriminator data from the SIFT chips to the Digital Boards.

A second PLL is used to multiply the beam crossing clock by nine to create the data rate clock for the Virtual SVX subsystem. Since the MCM has a total of 72 channels and the Virtual SVX must be read out using the byte-wide SVX data bus, this faster clock is required in order to pack all the discriminator bits up into bytes and keep up with the crossing rate.

The Clock Generator also uses silicon delay lines and CPLD logic to create all of the various clock signals required by the SIFT for operation. The crossing clock is sent through the delay lines and the leading edge of each delay tap is used to set and reset asynchronous latches in the CPLD, creating SIFT control clocks with 5nsec edge placement relative to each other and to the crossing clock. Various programs in the CPLD may be loaded to compensate for slight differences in fiber length and/or SVX Sequencer delays, insuring that the SIFT acquisition interval is properly timed with respect to the time when charge is delivered.

A more detailed analysis of the clock generator may be found at

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990105a.pdf

2.8. Multi-Chip Modules

The Multi-Chip Modules contain four SIFT custom ASICs which function as 18-channel discriminators and charge transfer switches. Each SIFT has an individual charge threshold setting. The timing clocks are common among all four SIFTs. When the charge is collected by the SIFTs the discriminator measurement is made when the Sample-and-Hold (S/H) switch is closed. An internal RC network and high-impedance buffer insure that the S/H result persists during the next crossing interval, allowing plenty of time for the CPLDs to latch the data. This same S/H signal also causes the charge to be copied – at a less than unity gain – onto a holding capacitor. A subsequent READ clock transfers the charge from all four SIFTs to an SVX IIe chip inside the MCM, which acts as a 128-channel, 8-bit charge sensitive ADC.

The SVX IIe implements an analog buffer such that charges collected from the SIFTs are held for up to 31 crossings until discarded. Should a trigger accept occur within the 31 crossings, the SVX IIe may then be placed into the Digitize and Readout modes in order to perform the actual A/D conversion. Since conversion occurs only upon demand, new charge may be placed into the chip every crossing until a conversion is required.

Each MCM is a large, 228 pin surface mount device which contains the five ASICs plus numerous resistors and capacitors on a high density printed circuit substrate. Each MCM is individually tested on a separate MCM Test Board prior to their being soldered onto the AFE boards. Precious little up-to-date information on the SIFT is available on the Web; contact the author for paper copies of documentation and/or SPICE models. The MCM itself was designed by Mike Matulik (matulik@fnal.gov) .

2.9. Virtual SVX Subsystem

The Virtual SVX subsystem utilizes a set of CPLDs which capture the discriminator data from the MCMs and buffers this data into small Event Delay FIFOs. These FIFOs provide the same amount of digital buffer depth as is provided by the analog buffer in the SVX IIe chip, such that when a trigger occurs, the discriminator pattern which caused the trigger may be read out in addition to the SVX IIe data of the event. The intent of this is to provide calibration information where the SVX IIe values can be compared against the SIFT discriminators, providing a cross-check of discriminator thresholds.

Each MCM has a 512 X 8 FIFO associated with it to handle this delay function. A CPLD with a dual 512 X 8 FIFO monitors the state of the SVX IIe chips. During normal acquisition, this CPLD counts clocks, and when the FIFO buffer depth is equal to the delay that's been programmed into the SVX IIe chips, it then maintains the FIFO depth at that point by issuing read clocks and discarding the data at the same rate that new data is put into the FIFOs. This insures that at all times the data at the outputs of the FIFOs is the digital data of interest. When the level 1 trigger accept signal is received, the SVX IIe chips enter a Digitize mode. During that same time interval the VSVX CPLD collects all the data from the eight Event Delay FIFOs and prepares the data for readout. After the Digitize cycle is complete the SVX IIe chips are read out. A token is passed from chip to chip (i.e. from MCM to MCM). When the token falls out of the last MCM, it goes to the Virtual SVX, which then reads out the discriminator data in a format compatible with the SVX IIe data.

A detailed analysis of the Virtual SVX system is available at

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a991015a.pdf

2.10. SVX Sequencer Interface

Initialization, control and readout of the SVX IIe chips in the MCM is accomplished by the SVX Sequencer, an external circuit board mounted in a rack near the AFE boards. A ribbon cable connection from the SVX Sequencer to the AFE provides the bidirectional data bus, required control signals and clocks.

The SVX Sequencer is the source of the master clock for the SVX IIe chips, and also the source of the beam crossing clock from which all SIFT timing is derived. The Level 1 Accept (the master trigger signal which initiates readout of the SVX IIe chips and the Virtual SVX) is also carried over this cable. The SVX Sequencer was designed by Mike Utes and documentation for this module may be found at

http://d0server1.fnal.gov/users/utes/default.htm

2.11. Analog Monitoring and Control

Various analog control circuits interface to the microprocessor, the DAC array and the MCMs in order to control the system. A couple of op-amps are used with each MCM in order to generate the mirror-image voltage of the threshold setting, as the SIFT threshold voltage is defined as the difference between two voltages centered about 2.5V, not a simple voltage with respect to the main return. In addition, a pair of op-amps per VLPC cable are used to create the constant current used to measure the temperature of the VLPC. A carbon composition resistor is used which is on the edge of superconductivity at the normal operating temperature of about 9

Kelvin. The voltage dropped across this resistor is measured using an instrumentation amplifier and this voltage is sensed by the A/D converter of the microprocessor through an analog mux. In similar vein, a power op-amp is used to drive a heater resistor should the VLPCs be too cold. Since the normal temperature of liquid helium is about 4.3 Kelvin, the heater resistor is expected to be used regularly. A bias voltage is also required for the VLPCs themselves, and this is driven by an op-amp from a DAC output. The voltage applied to the VLPCs is brought back to the microprocessor A/D, as is a measurement of the current being drawn by the VLPCs.

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990607a.pdf provides a more detailed analysis of this subsystem, and of how the VLPC temperature is maintained.

2.12. Data Multiplexing and Serial Links

The 512 bits of discriminator data obtained every 132 nsec must be transmitted a few feet to the Mixer System (or, for other fibers, directly to Digital Boards). Obviously, a massively parallel cable would be most impractical. To accomplish this transfer, a dual serialization scheme is employed. At each of the eight MCMs a CPLD takes the 64 bits of data and, using the 53 MHZ clock, creates seven 10-bit words every 132 nsec. The extra six bits are filled using board status and diagnostic information.

These eight 10-bit buses are combined in pairs to form four 20-bit buses. Each 20-bit bus is connected to an LVDS driver part which internally multiplies the 53 MHz clock by another factor of seven. The driver part takes a 21-bit input at 53 MHZ and sends it out as three data bits (plus a sync clock) at a rate of about 371 MHZ. Thus, each 128 bits of MCM data are transmitted over four differential pairs at this 371 MHZ rate. Four of these high-speed serial links are then capable of transmitting all 512 bits of MCM data, plus 48 bits of status information, every 132 nsec.

The 21st bit of each link is connected to the 7.6 MHz crossing clock so that the receiver of the four links may check synchronization between the links. Since the data to the LVDS drivers is presented at 53MHZ, the crossing clock should result in this bit being set one word out of every seven. For those interested in how the LVDS part works, the data sheet is available at

http://d0server1.fnal.gov/projects/triggerelectronics/procurement/cft%20axial/data%20sheets/SN65LVDS95.pdf

3. EMBEDDED & DIAGNOSTIC/DEVELOPMENT SOFTWARE

The AFE board utilizes embedded software in the on-board microprocessor to respond to commands from the external world that appear on the MIL-STD 1553 bus. Diagnostic software uses the embedded routines to gain access to the various features of the board. Diagnostic software has no direct control over the board; everything has to go through the microprocessor.

3.1. Embedded Software

All embedded software in the AFE microprocessor is written in assembly language. The PIC 14000 has a very simple language structure consisting of fewer than 40 mnemonics. The datasheet for the device is located at

http://d0server1.fnal.gov/projects/triggerelectronics/procurement/cft%20axial/data%20sheets/pic14000.pdf

which contains a complete description of the instruction set in Chapter 11.

3.1.1. Software Tools & Methodologies

The standard MPLAB assembler for Microchip PIC products is used. This assembler is available free of charge from Microchip at http://www.microchip.com. The source code for the PIC14000 is found on the D0 server at

http://d0server1/projects/triggerelectronics/cae/mcm_test/firmware/990830_jta/*.asm

Following modular program structure, numerous files are used to build the program. The MAINPROG.ASM file contains the main program and initialization routines. All other files handle particular I/O chores.

3.1.2. Description Of Embedded Software

The basic structure of the program is to initialize the ports of the microprocessor and then enter a polling loop where commands from the MIL-STD 1553 interface are handled. A jump table is implemented which provides access to various command handling routines based upon the eight-bit command code sent to the processor, as shown in this code fragment:

```
CMD0        GOTO POLL_CMD       ;since we require the commands to be non-zero,
;                                this is merely a placeholder.
;                                A command of zero exits the processing loop
;                                by going back to the poll routine.
CMD1        GOTO TEST_Q         ;create internal test charges using CREF & TREF
CMD2        GOTO SET_EVENT_DELAY      ;get data from user and sends to register
CMD3        GOTO NULL_CMD
CMD4        GOTO NULL_CMD
CMD5        GOTO TURNON_PS            ;command 5: turn on power supplies
CMD6        GOTO TURNOFF_PS           ;command 6: turn off the power supplies
CMD7        GOTO NULL_CMD
CMD8        GOTO NULL_CMD
CMD9        GOTO NULL_CMD
```

```
CMDA          GOTO UPDATE_AtoD    ;command a: read data from A/D converter, store in
DPRAM (disabled)
CMDB          GOTO NULL_CMD
CMDC          GOTO SET_DIG_CTL    ;command c: write control value to digital control
latch
CMDD          GOTO NULL_CMD
CMDE          GOTO NULL_CMD
CMDF          GOTO UPDATE_DAC           ;command f: copy data values from DPRAM to DAC
```

The number of commands which the microprocessor can support is limited only by the fixed code space of the microprocessor. The reader is reminded that the microprocessor code space is limited to the 4K words within the device itself; no expansion of program memory is possible by the addition of more RAM to the board.

3.2. Development & Diagnostic Software

Diagnostics for the AFE board are provided using a PC running a Visual Basic program or even just the Microsoft Office suite of programs with their Visual Basic for Applications (VBA) extension. Bob Angstadt of D0 (angstadt@fnal.gov) has written a DLL which allows PCs using either form of Visual Basic (and, presumably, Visual C as well) to utilize one of the Bit3 interfaces to gain access to an external VME subrack. This VME subrack may then use one of the VME-to-1553 interfaces available at the experiment to control the AFE. In similar vein, direct PC-to-1553 interfaces such as those from Ballard may be used.

Owen Payne and Paul Rubinov have created a Visual Basic program for use with the MCM Test Board which forms the core from which the AFE test program will be made.

3.2.1. Description Of Hardware Test Platform

AFE boards are tested by use of a separate “AFE Test Board”, which has not yet been manufactured. Based upon the MCM Test Board (rev. C, the “Meltronix” board), the AFE Test Board uses a series of JFET transistors to generate test charge pulses which are fed to the inputs of the AFE over the same cables as will be used in the real application. A copy of the same MIL-STD 1553 interface and microprocessor blocks used in both the MCM Test Board and the AFE is used on the AFE Test Board to provide an interface by which the amount of charge delivered to different inputs of the AFE may be programmed. The AFE Test Board is planned for summer 2000, to be designed by J. Anderson and M. Matulik.

Optionally, an SVX Sequencer may be used to control and read out the SVX IIe chips on the AFE. If the SVX Sequencer is not used hardware on the AFE may be used to generate a local crossing clock from an on-board crystal oscillator.

3.2.2. Description Of Software Test Platform

An upgraded version of the existent MCM Test Board program will be used to test the AFE. All of the main features will be maintained plus expanded diagnostics based upon the use of the Virtual SVX circuitry.

4. INTERFACE SPECIFICATIONS

The AFE board talks to the world through its connection to the AFE Backplane. This backplane provides power, connection to the SVX Sequencer, LVDS output and connection to MIL-STD 1553. Inputs to the board are through flex cables that connect at the bottom edge.

4.1. MIL-STD 1553 Interface

This interface has been previously discussed. The MIL-STD 1553 interface is a serial protocol carried on two wires, at a bit rate of approximately one bit per microsecond. Manchester encoding is utilized and decoded via a standard interface chip. A CPLD acts as the deserializer and interface to the dual-port RAM.

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990312a contains a brief description of the 1553 protocol which may be used to understand how this bus works. Numerous other web sites also discuss this bus, which is still in fairly wide use in the avionics industry.

4.1.1. Addressing Modes

The AFE responds only to subaddresses 0x10 and 0x11.

4.1.2. Data Cycles Types

Only normal data cycles (no broadcasts) are supported.

4.1.3. Register Descriptions

Subaddress 0x10 is an address pointer register which selects the address of the dual-port RAM which will be read or written by the first access to subaddress 0x11. The dual-port ram has an address range of 0x0000 – 0x1FFF. Any data written to bits 15, 14 or 13 of subaddress 0x10 will be ignored. Having written to subaddress 0x10, reads or writes to subaddress 0x11 access successive locations in the dual-ported memory. The RAM address loaded by the write to subaddress 0x10 is incremented with each data word read or written to subaddress 0x11, such that a 5-word read from subaddress 0x11 after writing a value of 0x100 to subaddress 0x10 would result in the data from RAM locations 0x100, 0x101, 0x102, 0x103 and 0x104 being supplied. Since the 1553 spec allows for up to 32 words of transmission per access to a given subaddress, a single access to subaddress 0x11 may transfer up to 32 words to the RAM.

4.2. SVX Sequencer Bus Interface

The SVX Sequencer communicates with the AFE through a ribbon cable which lands upon the AFE Backplane. One cable actually contains two SVX control buses, and the backplane splits the signals such that each SVX cable services two adjacent AFE boards. Each SVX bus connection provides the following signals:

- 8-bit bidirectional SVX data bus
- open-collector DVALID signal driven from AFE to SVX Sequencer
- Differential SVX Clock
- Differential Crossing Clock

- CHANGE_MODE, MODE0 and MODE1 control lines to SVX
- VCAL calibration voltage
- HDI_EN, FIRST_CROSSING, SYNC_GAP and CFT_RESET control signals

By and large the SVX Sequencer interface only controls the operation of the SVX IIe chips and the Virtual SVX logic of the AFE board. The discriminator function is essentially independent of the SVX operation, and data can still be driven out the LVDS cables even if the SVX Sequencer is disconnected. However, since the master timing of the AFE board is derived from the crossing clock as supplied on this cable, for the board to work as part of the detector system this link must be present and functional.

The design of the Virtual SVX provides for limited cross-coupling between the microprocessor and the SVX data bus such that SVX data may be sampled and read out over the MIL-STD 1553 bus and/or 1553 data appended to the SVX readout.

4.3. Front Panel I/O, Test & Monitoring

The AFE has no front panel due to mechanical constraints. Because of the AFE's left-right symmetric design, an AFE inserted on either side of the mechanical cassette will have a pad pattern for an unstuffed backplane connector at the 'front'. Various surface mount LEDs will be visible when the board is installed but none are specifically mounted on the board edge.

4.4. Rear Connector Interface

All AFE I/O occurs through the rear connector, to the backplane. The AFE connects to the backplane using two metric connectors from the series used for Compact PCI (e.g. AMP Z-Pack and/or equivalents from ERNI, FCI, etc.). One connector is a type 'A' which integrates 110 pins of connection with mechanical alignment features to insure the connector is aligned prior to pin mating. The other connector is a type 'B' which forfeits the alignment piece to provide 125 pins. Both connectors utilize top side shields which are used as extra ground returns.

4.4.1. Connector Pin Configurations

Table 1 shows the pinout for the AFE Backplane, for the Right-Handed insertion of the AFE board. The pinout for the Left-Hand insertion is, of course, swapped left-to-right. Different colors are used to highlight different groups of pins. The green pins are all grounds. The analog and digital ground planes of the AFE are tied together to the common backplane ground. The grey pins are reserved for use in the 12-MCM version of the AFE and are not connected in the 8-MCM AFE.

	F (Top Shield)	**E**	**D**	**C**	**B**	**A**	**Z (Bottom Shld)**
1	GND	5.5V	+3.3V	GND	1553-	1553+	GND(BP)
2	GND	5.5V	+3.3V	GND	SLOTBIT1	SLOTBIT2	GND(BP)
3	GND	5.5V	+3.3V	GND	SLOTBIT8	SLOTBIT3	GND(BP)
4	GND	+3.3V	+3.3V	GND	SLOTBIT7	SLOTBIT4	GND(BP)
5	GND	GND	GND	GND	SLOTBIT6	SLOTBIT5	GND(BP)
6	GND	LVDS1_D1+	LVDS1_D1-	GND	LVDS1_D2+	LVDS1_D2-	GND(BP)
7	GND	LVDS1_D0-	LVDS1_D0+	GND	LVDS1_CLK+	LVDS1_CLK-	GND(BP)
8	GND	GND	GND	GND	LVDS1_D3+	LVDS1_D3-	GND(BP)
9	GND	LVDS2_D1+	LVDS2_D1-	GND	LVDS2_D2+	LVDS2_D2-	GND(BP)
10	GND	LVDS2_D0-	LVDS2_D0+	GND	LVDS2_CLK+	LVDS2_CLK-	GND(BP)
11	GND	GND	GND	GND	LVDS2_D3+	LVDS2_D3-	GND(BP)
12	GND	LVDS3_D1+	LVDS3_D1-	GND	LVDS3_D2+	LVDS3_D2-	GND(BP)
13	GND	LVDS3_D0-	LVDS3_D0+	GND	LVDS3_CLK+	LVDS3_CLK-	GND(BP)
14	GND	GND	GND	GND	LVDS3_D3+	LVDS3_D3-	GND(BP)
15	GND	LVDS4_D1+	LVDS4_D1-	GND	LVDS4_D2+	LVDS4_D2-	GND(BP)
16	GND	LVDS4_D0-	LVDS4_D0+	GND	LVDS4_CLK+	LVDS4_CLK-	GND(BP)
17	GND	GND	GND	GND	LVDS4_D3+	LVDS4_D3-	GND(BP)
18	GND	LVDS5_D1+	LVDS5_D1-	GND	LVDS5_D2+	LVDS5_D2-	GND(BP)
19	GND	LVDS5_D0-	LVDS5_D0+	GND	LVDS5_CLK+	LVDS5_CLK-	GND(BP)
20	GND	GND	GND	GND	LVDS5_D3+	LVDS5_D3-	GND(BP)
21	GND	LVDS6_D1+	LVDS6_D1-	GND	LVDS6_D2+	LVDS6_D2-	GND(BP)
22	GND	LVDS6_D0-	LVDS6_D0+	GND	LVDS6_CLK+	LVDS6_CLK-	GND(BP)
23	GND	GND	GND	GND	LVDS6_D3+	LVDS6_D3-	GND(BP)
24	GND	GND	GND	GND	GND	GND	GND(BP)
25	GND	+12V	+12V	GND	-12V	-12V	GND(BP)
1	GND	DVALID B	GND	SYNC_GAP	GND	CROSSING*	GND(BP)
2	GND	GND	1st XING	GND	CROSSING	GND	GND(BP)
3	GND	SVX_DAT0B	GND	VCAL B	GND	PRIORITY_OUTB	GND(BP)
4	GND	GND	DIR B	GND	SVX_DAT2B	GND	GND(BP)
5	GND	SVX_DAT5B	GND	HDI_EN B	GND	SVX_DAT1B	GND(BP)
6	GND	GND	SVX_DAT3B	GND	SVX_DAT6B	GND	GND(BP)
7	GND	MODE1 B	GND	SVX_DAT7B	GND	SVX_DAT4B	GND(BP)
8	GND	GND	PRIORITY_INB	GND	CLK* B	GND	GND(BP)
9	GND	CFT_RESET	L1 ACCEPT	CLK B	GND	MODE0 B	GND(BP)
10	GND	CLAMP	GND	SPARE	CHG_MODE B	GND	GND(BP)
11	GND	+5V	+5V	+5V	+5V	+5V	GND(BP)
12							
13				KEY AREA			
14							
15	GND	DVALID B	GND	SYNC_GAP	GND	CROSSING*	GND(BP)
16	GND	GND	1st XING	GND	CROSSING	GND	GND(BP)
17	GND	SVX_DAT0B	GND	VCAL B	GND	PRIORITY_OUTB	GND(BP)
18	GND	GND	DIR B	GND	SVX_DAT2B	GND	GND(BP)
19	GND	SVX_DAT5B	GND	HDI_EN B	GND	SVX_DAT1B	GND(BP)
20	GND	GND	SVX_DAT3B	GND	SVX_DAT6B	GND	GND(BP)
21	GND	MODE1 B	GND	SVX_DAT7B	GND	SVX_DAT4B	GND(BP)
22	GND	GND	PRIORITY_INB	GND	CLK* B	GND	GND(BP)
23	GND	CFT_RESET	L1 ACCEPT	CLK B	GND	MODE0 B	GND(BP)
24	GND	CLAMP	GND	SPARE	CHG_MODE B	GND	GND(BP)
25	GND	+5V	+5V	+5V	+5V	+5V	GND(BP)

Table 1

4.4.2. Signal Descriptions

The various LVDS +/- signals are 370 MHz, Low-Voltage Differential Signaling standard, differential current source signals. They drive differential transmission lines and expect to see a termination equal to the characteristic impedance (typically 100 ohms) across the pair at the receiving end. The SLOTBIT signals are either left floating or tied to GND in order to give each AFE board a unique address for purposes of 1553 communication. The bits are a combination of slot position and a backplane address such that every AFE in the Central Fiber Tracker has a unique 1553 RT address.

All SVX signals are TTL level signals. All are inputs to the AFE except for DVALID and the SVX data bus. DVALID is an open-collector output from the AFE, and the SVX data bus is bidirectional.

4.4.3. Protocols

The LVDS data is continuous transmission with the data carried on the three data bits and the PLL of the LVDS receiver synchronized using the CLK lines in each link. Data on the LVDS links consists of 'frames', where one 'frame' is transmitted every 132 nsec. Each 'frame' consists of seven words of data. The most significant bit of the parallel data word issued by the receiver chip is used for synchronization, and is a copy of the crossing clock (high for one word, low otherwise). This acts as the 'start bit' for the frame.

SVX protocol consists of placing the SVX chip in one of four modes (Initialize, Acquire, Readout or Digitize) via use of the CHANGE_MODE, MODE0 and MODE1 lines. Dependent on mode, the SVX bus may be a data bus or individual control lines. The clock also changes speed in different modes. Please refer to the SVX II "Beginner's Guide" which may be found at

http://www-ese.fnal.gov/eseproj/svx/svx_htm/bgtsvx.htm

This document describes the 'generic' SVX II. Some variations are present in the SVX IIe, but they are minor.

4.5. Daughterboard Interface

The 8-MCM AFE has no daughterboard but the 12-MCM AFE does. This will be described in a different document. The daughterboard is expected to mount close to the motherboard in the 12-MCM configuration, utilizing the Samtec OPC series of connectors.

5. ELECTRICAL & MECHANICAL SPECIFICATIONS

5.1. Packaging & Physical Size

The AFE is 14.435 inches high by 19.25 inches wide. It is a bare circuit board with no front panel. Components are mounted on both sides. Due to mechanical restrictions, component height above the board may be no more than 0.431" on the component side and no more than 0.050" on the solder side.

5.2. PC Board Construction

Ten layer FR4 construction is used. Some gold plating is on the component side where the flex cables land.

5.3. Power Requirements

Spreadsheet calculations indicate that the power dissipation should be approximately 34 Watts, split between +5V, +3.3V, and ± 12V. Local power regulation at each MCM insures minimal noise.

5.4. Cooling Requirements

50 CFM airflow is provided by fans mounted below the backplane, providing airflow front-to-back. Normal bottom-to-top airflow is unavailable because the bottom is blocked by the cryostat and the top by the fiber optic cables entering the cassette.

6. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

Typical protection features such as temperature monitoring and power supply fusing are present on the AFE. The critical analog components are further insulated from power supply transients by the use of on-board linear regulators. Power dissipation has been minimized such that no component will dangerously overheat (e.g. to points of combustion) even if the fans fail; unassisted convection tests of physical heat models show that the air exit out the front is wide enough to accomplish this.

6.1. Module Fusing & Transient Supression

All power supplies entering the AFE from the backplane are fused and have transient suppressors.

6.2. Other Safety & Quality Assurance Subsections

The local microprocessor contains a built-in temperature sensor and continuously reports the temperature of the board. Bulk power supplies are remotely sensed at the backplane. The microprocessor also continuously monitors and controls the cryostat temperature.